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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/772,750	02/04/2004	Koichi Yamada	P18129	5683
59796	7590	11/15/2010	EXAMINER	
INTEL CORPORATION			GEIB, BENJAMIN P	
c/o CPA Global				
P.O. BOX 52050			ART UNIT	PAPER NUMBER
MINNEAPOLIS, MN 55402			2181	
			NOTIFICATION DATE	DELIVERY MODE
			11/15/2010	ELECTRONIC

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

heather.l.adamson@intel.com

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/772,750	YAMADA ET AL.	
	<b>Examiner</b>	<b>Art Unit</b>	
	BENJAMIN P. GEIB	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) Responsive to communication(s) filed on 04 June 2010.  
 2a) This action is **FINAL**.                    2b) This action is non-final.  
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) Claim(s) 1-28 is/are pending in the application.  
 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
 5) Claim(s) \_\_\_\_\_ is/are allowed.  
 6) Claim(s) 1-28 is/are rejected.  
 7) Claim(s) \_\_\_\_\_ is/are objected to.  
 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) The specification is objected to by the Examiner.  
 10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
 a) All    b) Some \* c) None of:  
 1. Certified copies of the priority documents have been received.  
 2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)  | Paper No(s)/Mail Date. _____ .                                    |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date <u>05/12/2010</u> . | 5) <input type="checkbox"/> Notice of Informal Patent Application |
|   | 6) <input type="checkbox"/> Other: _____ .                        |

## DETAILED ACTION

### ***Response to Arguments***

1. Applicant's arguments, see Pre-Brief Conference Request, filed 06/04/2010, with respect to the rejection(s) of claim(s) 1, 10, 15, and 20 under 35 U.S.C. 102(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of newly found prior art, Nemirovsky et al., U.S. Patent No. 6,389,449.

### ***Claim Rejections - 35 USC § 102***

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-8 and 10-27 are rejected under 35 U.S.C. 102(b) as being anticipated by Nemirovsky et al., U.S. Patent No. 6,389,449 (hereinafter Nemirovsky).

4. Referring to claim 1, Nemirovsky has taught a method comprising:

in a processor based system where a plurality of logical processors [*The processor has a plurality of contexts (called streams), which are logical processors*] of a single physical processor [*one physical processor; See FIG. 1A*] share processor execution resources of the single physical processor [*Functional Resources; FIG. 1A, component 107*], in response to a first logical processor in the plurality of processors being scheduled to enter an idle state due to lack of scheduling tasks, making a processor execution resource previously reserved for the first logical processor available to any of the plurality of logical processors [*The streams have reserved resources (See FIG. 1C; column 6, lines 41-46) and can change their resources according to their needs (column 9, lines 49-53). Therefore, when a stream is idle it makes the resources previously reserved for it available to the other streams (i.e. logical processors)*].

Art Unit: 2181

5. Referring to claims 2 and 21, taking claim 2 as exemplary, Nemirovsky has taught the method of claim 1 further comprising reserving the processor execution resource for the first processor in response to the first processor being scheduled to execute a task *[column 6, lines 33-47]*.

6. Referring to claims 3 and 22, taking claim 3 as exemplary, Nemirovsky has taught the method of claim 2 wherein each of the plurality of processors is a logical processor of the processor based system *[column 4, lines 48-60]*

7. Referring to claims 4, 11, 16, and 23, taking claim 4 as exemplary, Nemirovsky has taught the method of claim 3 wherein the first processor being scheduled to enter an idle state further comprises the first processor executing a processor instruction requesting the first processor to enter an idle state *[the stream executes an instruction that puts it to sleep (i.e. idle); column 10, lines 55-64]*

8. Referring to claim 5, 12, 17, and 24, taking claim 5 as exemplary, Nemirovsky has taught the method of claim 4 wherein making the processor execution resource previously reserved for the first processor available to any of the plurality of processors further comprises releasing the processor execution resource into a common pool of processor execution resources *[making the previously reserved resource available comprises modifying the resource assignment bitmap, thereby releasing the resource into a common resource pool; column 6, lines 29-47]*.

9. Referring to claims 6 and 25, taking claim 6 as exemplary, Nemirovsky has taught the method of claim 2 wherein the first processor being scheduled to execute a task further comprises the first processor receiving a wake up signal *[An idle thread receives a wake up signal from the supervisor thread to execute a task; column 10, lines 22-34]*.

10. Referring to claims 7, 13, 18, and 26, taking claim 7 as exemplary, Nemirovsky has taught the method of claim 6 wherein the processor execution resource previously reserved for the first processor further is statically allocated to the first processor *[column 6, lines 48-57]*; and wherein releasing the processor execution resource into a common pool of processor execution resources further comprises de-allocating the processor execution resource from the first processor *[releasing the resource into a common resource pool comprises deallocating the resource using the resource assignment bitmap; column 6, lines 29-47]*.

Art Unit: 2181

11. Referring to claim 8, 14, 19, and 27, taking claim 8 as exemplary, Nemirovsky has taught the method of claim 6 wherein the processor execution resource previously reserved for the first processor is locked by the first processor [*reserved resources are indicated as locked by the resource assignment bitmap; column 6, lines 29-47*]; and wherein releasing the processor execution resource into a common pool of processor execution resources further comprises unlocking the processor execution resource processor [*releasing the resource into a common resource pool comprises unlocking the resource by modifying the resource assignment bitmap; column 6, lines 29-47*].

12. Referring to claim 10, Nemirovsky has taught a processor comprising:

A single physical processor [*one physical processor; See FIG. 1A*] that implements a plurality of logical processors [*The processor has a plurality of contexts (called streams), which are logical processors*]; and logic to execute an instruction set which when executed by a first logical processor, cause the first logical processor to make a processor execution resource previously reserved for the first processor available to a second processor in the plurality of processors in response to the first logical processor being scheduled to enter an idle state due to lack of scheduling tasks [*The streams have reserved resources (See FIG. 1C; column 6, lines 41-46) and can change their resources according to their needs (column 9, lines 49-53). Therefore, when a stream is idle it makes the resources previously reserved for it available to the other streams (i.e. logical processors)*].

13. Referring to claim 15, Nemirovsky has taught a system comprising: a physical processor [*one physical processor; See FIG. 1A*], the processor comprising: a plurality of logical processors [*The processor has a plurality of contexts (called streams), which are logical processors*] implemented in the physical processor; and an instruction set, the instruction set comprising one or more instruction which when executed by a first logical processor, cause the first logical processor to make a processor execution resource previously reserved for the first processor available to a second processor in the plurality of processor in response to the first logical processor being scheduled to enter an idle state due to lack of scheduled tasks [*The streams have reserved resources (See FIG. 1C; column 6, lines 41-46) and can change their resources according to their needs (column 9, lines 49-53). Therefore, when a stream is idle it makes the resources previously reserved for it available to the other streams (i.e. logical*

Art Unit: 2181

*processors}); firmware to schedule the first logical processor to enter an idle state [the master thread is firmware (column 8, lines 15-30) thread that can put streams to sleep (i.e. idle) (column 7, lines 47-65)]; and a bus to interconnect the firmware and the processor [See bus connecting instruction memory with processor; FIG. 1A].*

14. Referring to claim 20, Nemirovsky has taught a machine accessible medium having stored thereon data which when accessed by a machine cause the machine to perform a method, the method comprising: in a processor based system where a plurality of logical processor [*The processor has a plurality of contexts (called streams), which are logical processors*] implemented in a single physical processor [*one physical processor; See FIG. 1A*] share processor execution resources of the physical processor [*Functional Resources; FIG. 1A, component 107*], in response to a first logical processor in the plurality of logical processor being scheduled to enter an idle state due to lack of scheduled tasks, making a processor execution resource previously reserved for the first logical processor available to a second logical processor in the plurality of processors [*The streams have reserved resources (See FIG. 1C; column 6, lines 41-46) and can change their resources according to their needs (column 9, lines 49-53).* Therefore, when a stream is idle it makes the resources previously reserved for it available to the other streams (i.e. logical processors)].

#### ***Claim Rejections - 35 USC § 103***

15. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

16. Claims 9 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nemirovsky.

17. Referring to claims 9 and 28, taking claim 9 as exemplary, Nemirovsky has taught the method of claim 5 wherein the common pool of processor execution resources comprises a variety of processor

Art Unit: 2181

resources [Nemirovsky; column 23-32]. Nemirovsky has not explicitly taught that the pool comprises a translation lookaside buffer and the processor execution resource is a translation cache entry from the translation lookaside buffer. However, it would have been obvious to one of ordinary skill in the art to modify Nemirovsky so that the pool of common resources would include a translation lookaside buffer and the resource would be a translation cache entry from the translation lookaside buffer. The motivation for doing so would have been to allow translation lookaside buffer entries to be shared among streams as needed.

### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to BENJAMIN P. GEIB whose telephone number is (571)272-8628. The examiner can normally be reached on Mon-Fri 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alford Kindred can be reached on (571) 272-4037. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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